# ELEC 305 - Digital Systems Design Laboratory

Fall 2024 - Syllabus

## Description

Hardware description languages, digital logic synthesis, combinational logic, arithmetic logic, sequential logic, memory and control units, computer organization. Field Programmable Gate Arrays (FPGA). Laboratory work, design project.

## Content

A hands-on course introducing state-of-the-art digital design workflows and how to use them for realizing higher-level hardware applications (we will build circuits, not software/programs!). First part of the course focuses on the fundamentals, where topics include the standard workflow (design, verification, synthesis, and implementation), Hardware Description Languages (Verilog, VHDL), Field Programmable Gate Array (FPGA) structures, common combinational and sequential logic blocks, RTL (Register Transfer Level) design, constraints, analyses and optimizations. Second part of the course focuses on interfacing these digital systems with signals in the physical world and building circuits on FPGAs to process those signals with DSP and neural-network based algorithms. Topics in this part include number representations (primarily fixed point) and bit-accurate simulation of the algorithms under arithmetic constraints in software, and realization of common operators used by such algorithms (e.g., FIR filters, neural network layers) in hardware. The Vivado Design Suite, Xilinx/AMD FPGAs and VHDL will be employed for labs and projects throughout the semester.

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|---|---|
| **Days & Times:** | TuTh 4:00PM - 5:10PM + Th 5:30PM - 6:40PM |
| **Room(s):** | SNA B220 |
| **Instructor / Email:** | Burak Soner / bsoner@ku.edu.tr |
| **TAs / Office Hours:** | No TAs / Th 3:00-4:00PM, ENG B10, by appointment |
| **Credits / ECTS Credits:** | 3 / 6 |
| **Prerequisites:** | ELEC 205, consent of the instructor |
| **Language:** | English |
| **Course website:** | https://www.buraksoner.com/elec305 (activated after the 1st lecture) |

## Objectives / Learning Outcomes

- Introduction to the concept of digital system design over hardware description languages as opposed to design on pen-and-paper, and its differences from software programming.
- Providing hands-on experience with VHDL and professional digital design tools such as the Vivado Design Suite and Xilinx/AMD FPGAs.
- Bridging the gaps between digital systems design, sensing technologies, DSP and state-of-the-art AI-ML methods to motivate further research at their intersections.
- Motivating students towards building tools for their own personal, research or commercial use via cost-efficient digital systems.

## Teaching Methods

- The regular meeting times are divided between in-class teaching sessions (lectures) and lab sessions, which alternate throughout the semester. In-class teaching covers the basics to enable lab work.
- 75% attendance is mandatory for both lab sessions and lectures (separately). Failure to adhere without justification will result in an automatic failure (F).
- A term project that involves designing and building a working digital system on an FPGA will be required. Documentation (reporting) and implementation will both be evaluated.
- Labs will utilize Xilinx/AMD FPGA hardware and the Vivado Design Suite. Hardware will be provided by the instructor and the Vivado version installed in the computer labs will be used during the lab sessions. Students need to submit reports after each lab session.
- VHDL homeworks will be assigned to help the students familiarize with the language. Students will also be able to install Vivado on their PCs to familiarize themselves and for use in their term project since it's free software. The instructor will provide support.
- The course has only a single exam: the final exam. It will consider all topics and focus on evaluating the engineering knowledge and skill gained throughout the semester.

## Assessment Methods and Grading

- Attendance: 0%, but attendance to 75% of all sessions is mandatory
- VHDL Homeworks: 20%
- Laboratory Tasks: 30%
- Term Project: 35%
- Final Exam: 15%

## Workload Breakdown

| Work | Description | Total Hours per semester |
|---|---|---|
| Lectures | In-class teaching sessions | 15 |
| Homeworks | Working on VHDL assignments | 20 |
| Labs | Laboratory sessions | 25 |
| Labs | Preparation and writing reports for the labs | 35 |
| Project | Project implementation and documentation | 45 |
| Project | Preparation for the project presentation | 10 |
| Exam | Preparation for the final exam | 30 |
| **Total workload** | | **180** |

## Schedule

| Sessions | Content |
|---|---|
| Lecture Set 1 | Course logistics and overview |
| Lecture Set 2 | Revisiting fundamentals: Digital computing, combinational and sequential, FPGA structure and HDLs |
| Tutorial 1 | Getting Started with Vivado and VHDL |
| Lab 1 | Standard digital design workflow, counters, boolean circuits |
| Lecture Set 3 | System verification, simulation, preparing testbenches |
| Tutorial 2 | Designing testbenches and simulating circuits during development |
| Lab 2 | FSM design, implementation and verification |
| Lecture Set 4 | Analysis & Optimization: constraints, pipelining, balancing |
| Lecture Set 5 | FPGA I/O, interfaces and communication protocols |
| Lecture Set 6 | Number representations, fixed pt. arithmetic, quantization artifacts |
| Lecture Set 7 | Common FPGA blocks in DSP and their software simulations |
| Lab 3 | DSP algorithms on FPGAs |
| Lecture Set 8 | Common FPGA blocks in AI / ML and their software simulations |
| Lab 4 | Neural networks on FPGAs - A simple regression task |

## Resources / Links

The lecture slides are the main resource since a single book does not cover all materials in this course. However, the following are also useful resources:

*Digital Design with RTL Design*, VHDL & Verilog, 2nd Edition, by F. Vahid, Wiley.
*Digital Design and Computer Architecture*, 2nd Edition, by Harris & Harris, Morgan Kaufmann.

**Links**
https://web.eecs.umich.edu/~valeria/research/thesis/thesis2.pdf
https://docs.xilinx.com/v/u/en-US/dh0002-vivado-design-flows-overview-hub
https://www.fpga4student.com/ (community effort, not always reference-worthy)
https://www.youtube.com/@marcowinzker3682/videos - YouTube channel on FPGAs and NNs
https://www.youtube.com/playlist?list=PLZv8x7uxq5XY-IQfQFb6mC6OXzz0h8ceF (VHDL tutorial)

## Academic Dishonesty

Koç University expects all its students to perform course-related activities in accordance with the rules set forth in the Student Code of Conduct 1. Actions considered as academic dishonesty at Koç University include but are not limited to cheating, plagiarism, collusion, and impersonating. This statement's goal is to draw attention to cheating and plagiarism related actions deemed unacceptable within the context of Student Code of Conduct: All individual assignments must be completed by the student himself/herself, and all team assignments must be completed by the members of the team, without the aid of other individuals. If a team member does not contribute to the written documents or participate in the activities of the team, his/her name should not appear on the work submitted for evaluation.

Plagiarism is defined as "borrowing or using someone else's written statements or ideas without giving written acknowledgement to the author". Students are encouraged to conduct research beyond the course material, but they must not use any documents prepared by current or previous students, or notes prepared by instructors at Koç University or other universities without properly citing the source. Furthermore, students are expected to adhere to the Classroom Code of Conduct2 and to refrain from all forms of unacceptable behavior during lectures. Failure to adhere to expected behavior may result in disciplinary action.

There are two kinds of plagiarism: Intentional and accidental. Intentional plagiarism (Example: Using a classmate's homework as one's own because the student does not want to spend time working on that homework) is considered intellectual theft, and there is no need to emphasize the wrongfulness of this act. Accidental plagiarism, on the other hand, may be considered as a "more acceptable" form of plagiarism by some students, which is certainly not how it is perceived by the University administration and faculty. The student is responsible from properly citing a source if he/she is making use of another person's work. For an example on accidental plagiarism, please refer to the document titled "An Example on Accidental Plagiarism". If you are unsure whether the action you will take would be a violation of Koç University's Student Code of Conduct, please consult with your instructor before taking that action.

https://apdd.ku.edu.tr/en/academic-policies/student-code-of-conduct-2/
https://vpaa.ku.edu.tr/academic/classroom-code-of-conduct