ELEC 305

Digital System Design Lab

Fall 2024

Lecture 1:

Course Overview and Logistics

Outline

- About me
- Course Content
- Course Logistics
- Your inputs

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About me

- Koç Primary and High School (1998-2010)
- BSc: Sabancı University, Mechatronics (2014)
- PhD: Koç University, ELEC (2022) → ELEC491 TA for 5 years
- 10+ years of professional and research experience on power electronics, wireless sensing, scientific computing and edge AI
- Recent: R&D Manager @ HyperbeeAI (a.k.a. ShallowAI), continuing research at my own company + KU, lecturing at KU ELEC
- Trying to strengthen the academia-industry "bridge" in TR over *energy-autonomous wireless sensing and AI-based edge computing*
- Enthusiastic about remote sensing app.s and novel computing hardware
- Office hours: Th 3:00PM - 4:00PM @ ENG B10, by appointment

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Course content

- Hands-on course (85%: lab work) on **skills** for designing and deploying practical digital circuits
- Using a “hardware description language” (HDL) instead of prototyping on breadboards etc.

  → HDLs do not describe **programs** (like in Python, C, …), they describe **circuits** (we’ll focus on digital ones)
- Deploying circuits you describe in HDL to “Field Programmable Gate Array” (FPGA) hardware

  → You can think of FPGAs like embedded microprocessors (MCUs, like Arduino), but while MCUs run programs (software), FPGAs configure internal blocks to realize circuits (hardware)

  → Informative example: you can build a custom MCU circuit on the FPGA (google “Microblaze”) and later load a program onto that just like in an MCU. The FPGA simply carries the MCU circuit here
- Labs will consider signal processing and machine learning applications, but we will also see other widespread uses of digital circuits in the industry (e.g., “glue logic”, custom comm protocols, …)
- While we will study HDLs, this whole course will not be a tutorial for them, we’ll rather build things using an HDL as a tool for designing / testing circuits and we’ll learn it during the process.

Course content

Topics in Part I - Fundamentals:

- Brief review of digital systems and their fundamentals (combinational and sequential logic blocks etc.)
- FPGA structures and Hardware Description Languages (Verilog, VHDL, …) ⟶ we'll mostly practice VHDL
- RTL (Register Transfer Level) design and the design workflow (design, verification, synthesis, and implementation)

Topics in Part II - Applications on FPGAs:

- Interfaces, number representations (fixed point) and designing "FPGA-friendly" algorithms / systems
- Bit-accurate simulation of arithmetic constraints for testing algorithms before deployment
- Realizing common DSP and/or neural network (NN) blocks on FPGAs (e.g., FIR filters, "Linear" layers)

Other Topics (if time allows) **- Current Practices and Future Trends:**

- Industry practices (IP integration, HLS), the future of FPGAs, and of digital systems design research

Course content

In short …

Part I ⟶ Learn how to design and deploy digital circuits on FPGAs

Part II ⟶ Learn how to realize useful applications with them

Other Topics ⟶ Learn about the associated state-of-the-art use cases and research challenges

Course content

Labs & Tutorials (tentative)

→ Tutorial: Vivado / VHDL quickstart and examples

1. Simple combinational and sequential logic → counters, boolean functions

→ Tutorial: Simulation and testbenches in VHDL

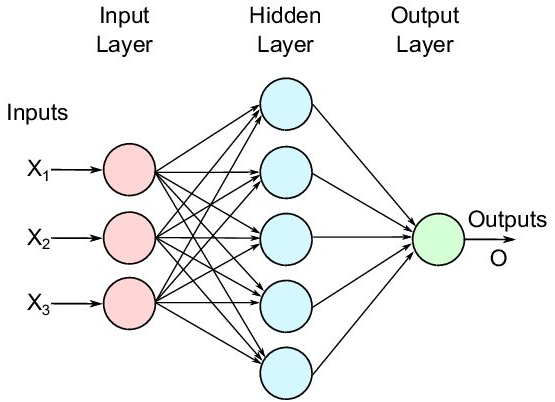
2. Finite state machines → Design and implement an FSM (e.g., digital combination lock)

3. Digital signal processing on FPGAs → FIR filtering

4. Neural networks on FPGAs → regression (e.g., california housing prices problem)

Course content

- The labs are a good demonstration of what this course will teach you to design and build:
- In lab 3 we'll work an arithmetic logic (multiply accumulate: "MAC") on the FPGA with a convolution operator and filter signals with it (recall: conv ↔ FIR filtering!)
- In lab 4, we will use that MAC unit to build a multi-layer perceptron (MLP) neural network circuit that takes takes inputs and does predictions on hardware (not Python!).
- We will be using pre-trained neural networks (or I will provide the training source code) that use custom fixed point number representations (like 7-bit numbers).
- Example: this is basically what chipmakers (e.g., Analog Devices) do early on during their development of custom chips (e.g., ADI: MAX7800) to verify their digital design on FPGAs before production



Course content

Term Projects

- The project topic is not set, students prepare their own proposals and negotiate with the instructor
- There are many great project examples on the MIT 6.111 course website that you can check out:

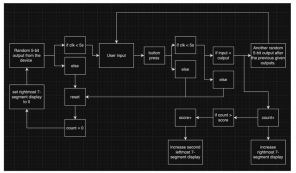
  https://web.mit.edu/6.111/volume2/www/f2019/ (see “Past projects - all”)

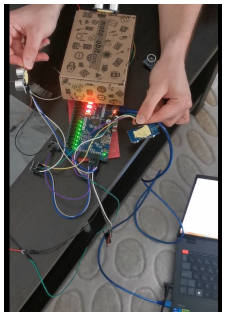
- These are typically challenging signal (audio or image) processing and/or game-based projects
- Since this is the 2nd semester of our course, we don’t have as many boards, interface modules and infrastructure capabilities, but we can purchase modules if you have exciting proposals for them!
- We already have a few audio IO modules and accelerometers as well as FPGA boards that you can use for the projects, I’ll provide mode details on them later

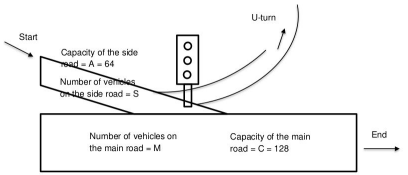
Course content

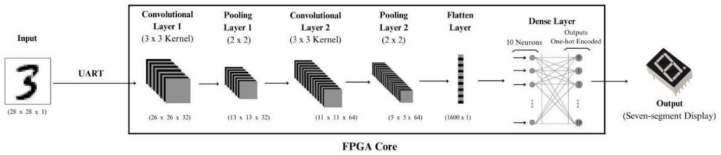
ELEC 305 projects last semester (S24)

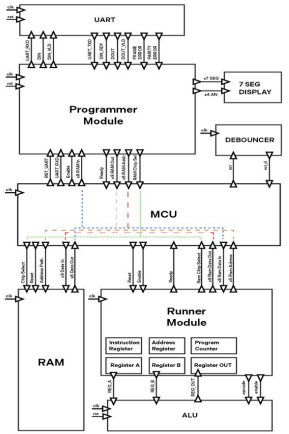
- Custom CPU
- JPEG decoder
- Traffic jam control and monitoring
- Car parking aid
- MNIST classifier (CNN)
- Simon says (game engine)

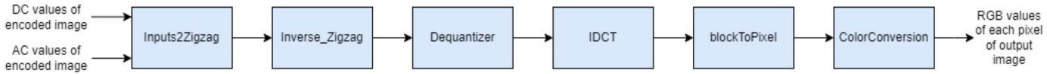








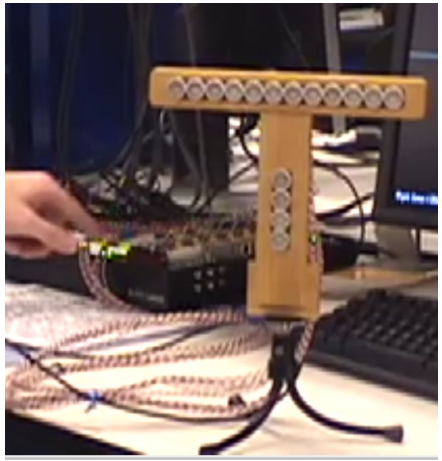


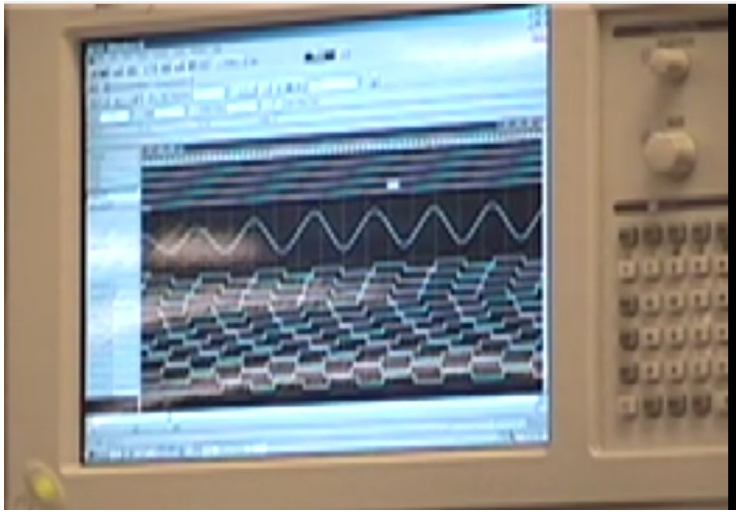


Course content

Some example projects from the MIT course (2005 - 2019)

- Digital SONAR





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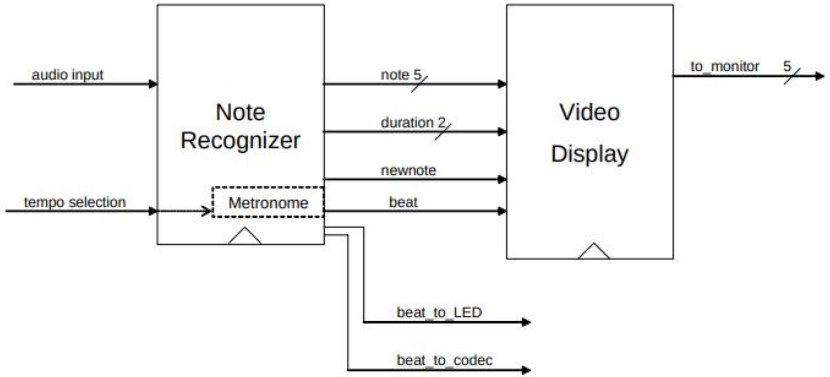
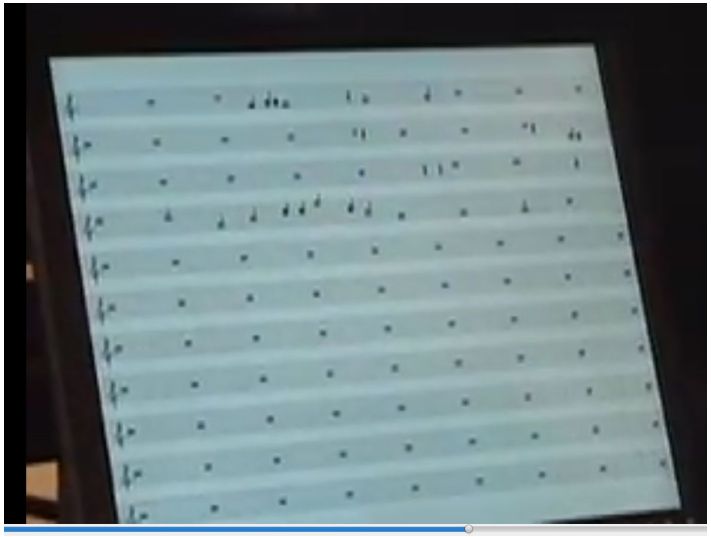
Some example projects from the MIT course (2005 - 2019)

- Music Transcriber ⟶ listens to music on the mic and writes closest musical notes on a sheet





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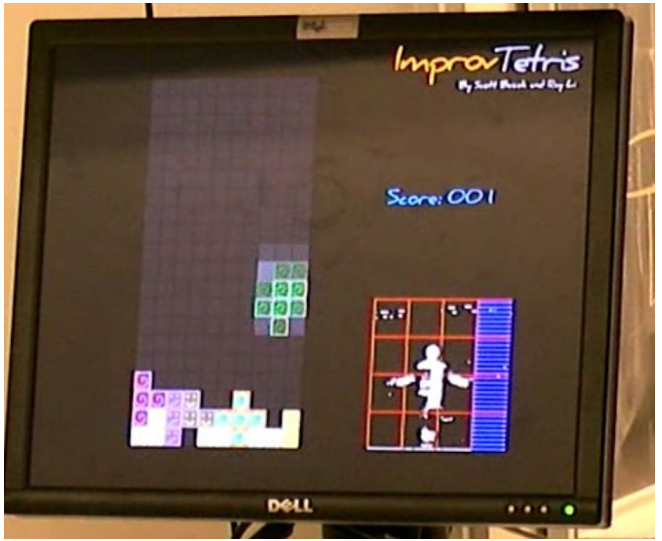
Some example projects from the MIT course (2005 - 2019)

- Improv Tetris ⟶ computer vision



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Course Logistics - Meeting Room

- All sessions are in SNA B220, see the [classroom IT website] for more info

Course Logistics - Sessions, Attendance

- We have 3 hrs/wk booked, but we will not have 3 sessions every week, I'll send early notifications

- There will be 2 lab tutorials and 4 lab sessions throughout the semester, the rest will be lectures or "support hours" in which I will provide hands-on support for your projects and general questions.
- Attendance rule: 75% for lab sessions and lectures **separately**. Tutorials are mandatory.
- Failure to attendance rules without justification → **direct F.**

Course Logistics - Attendance, Grading

- Further clarification on the attendance rule:
  - the lab tutorials are mandatory, not part of the 75% rule, everyone on the class roster must attend
  - the support hours are not office hours and they're not part of the 75% rule, they are not mandatory
  - please do not come in late or leave early unless it's absolutely unavoidable
    (I'm aware of the logistics problems on campus, but please plan accordingly, I certainly do!)
- Grading:
  - Attendance 0% contribution, but the 75% rule still holds
  - VHDL Homeworks 20%
  - Labs 30%
  - Project 35%
  - Final Exam 15%

Course Logistics - Labs, Hardware

- We have enough boards for everyone, so you will work on your own throughout the semester, …
- but I will encourage you to form groups of 3 as study partners because projects will be group work.
- So your lab and HW submissions still need to be your original work, but peer support is OK.
- We'll use the Basys3 boards for the labs, and we also have a few Cmod A7-35T units for projects
- These are both based on the Xilinx (now AMD) Artix-7 series FPGAs, if you want to check them out.
- I will provide some interface modules for your projects, such as microphones (electret + small pre-amp), audio IO and accelerometers. You can use these for processing physical signals.

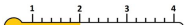
Course Logistics - Software, Access

- We will use the “Vivado Design Suite” by Xilinx (now AMD) to program the boards
- Vivado is HUGE (AMD Unified Installer for FPGAs & Adaptive SoCs 2023.2 SFD (TAR/GZIP - 103.92 GB)) , so I got them set up on B220, but you’re free to install it on your own PC.
- If you are using a Linux distro on your PC and want to install Vivado, I can help you out. I unfortunately don’t have experience in Win/Mac with this, but you can still ask, I’ll try my best.
- It would be ideal if we could give you some small FPGA boards for the whole semester so you can explore them, but we unfortunately cannot do that directly (zimmetleme problems). Contact me if you want to borrow hardware outside class hours, we can arrange this on a case-by-case basis.
- Course website: https://www.buraksoner.com/elec305 and https://github.com/sonebu , I’ll explain which one is for what later

Course Logistics - Term Project

- Term projects ⟶ Each group will submit a proposal and start working on it once it gets accepted.
- 2 proposal deadlines, you'll get 1 chance at a proposal revision by me and you have to have a proposal accepted by the second deadline or you unfortunately lose 35% of the course grade. Earlier is OK.
- Challenging projects will receive higher credit. To facilitate this, each project will be issued a "challenge point" (CP) between 1 and 4. The CP of your project will modulate your 35% project grade as follows:

- CP = 1 ⟶ your project can get max. 20% out of the 35%



- CP = 2 ⟶ your project can get max. 25% out of the 35%

- CP = 3 ⟶ your project can get max. 30% out of the 35%

- CP = 4 ⟶ your project can get max. 35% out of the 35%

- I will provide suggestions during the proposal phase to push all projects up to CP=4, but it's your choice

Course Logistics - Term Project

- Each group will do a short presentation after report submission. Group members will describe their contributions. A significant part of the evaluation will be on this presentation and the report.
- We'll have "support hours" in some of our planned sessions. I'll help you with different aspects of your projects during these hours
- Support hours do not have mandatory attendance, but please let me know if you're coming so that I don't keep waiting if no one is coming
- Support hours schedule:
    1. Proposals
    2. Proposals and project implementation
    3. Project implementation
    4. project implementation and reports

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Your inputs

- Any questions?
- Why are you planning on taking this course?
- What are your expectations from this course, what do you expect to learn?
- Any specific topic that you're relatively more interested in?
- Anyone with previous experience in digital design, an HDL, FPGAs, …?
- Any ideas for a project? We can test a few right now

next → revisiting fundamentals